



## JTAG-based UEFI Debug and Trace

**UEFI 2020 Virtual Plugfest** 

July 14, 2020

Presented by Alan Sguigna, ASSET InterTech, Inc.

### Meet the Presenter





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## Agenda

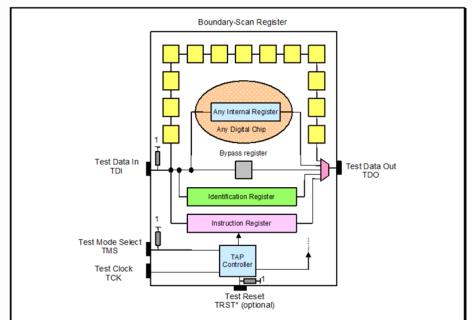




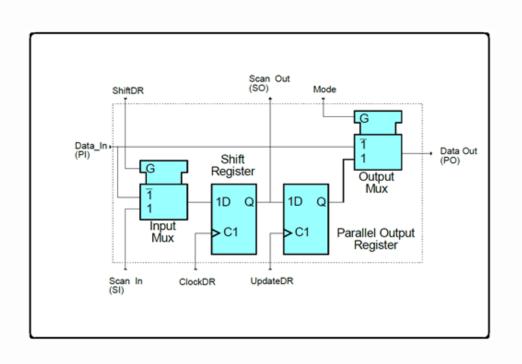
- What is JTAG? Debug use case
- Access mechanisms (platform-dependent)
- Tools of the Trade: Run-control, Trace, scripting
- Examples/ Demo:
  - Run-control: halt, go, single-step, breakpoint
  - Trace: Last Branch Record (LBR), Branch Trace
     Store (BTS), Instruction Trace, Architectural Event
     Trace, ME trace
  - Intel CScripts
- Call to Action

### What is JTAG?

- Celebrated its 30<sup>th</sup> Anniversary on February 15, 2020
- "Joint Test Access Group"
- IEEE 1149.1 and subsequent standards ingrained within much of today's commercial silicon
- Specifies a dedicated debug port with a serial communications interface
- Test Access Port implements a stateful protocol with test registers that connect with a chip's system logic
- An "engine" within chips that drives embedded instrumentation for a plethora of applications







## JTAG Applications



#### **Test**

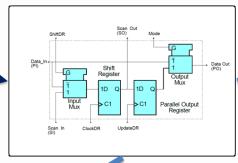
**Boundary-**Scan Test, JTAG-based functional test

#### Debug

Run-control (Intel ITP, AMD HDT, Arm CoreSight)

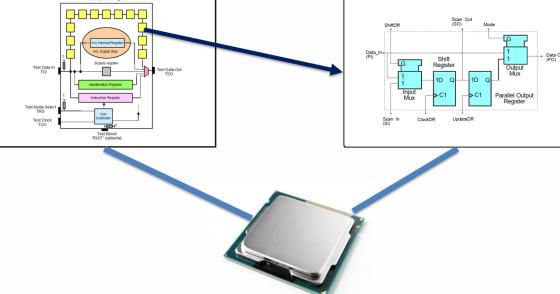
### **Validation**

Hardware performance / conformance



#### **Programming**

SVF, STAPL, JAM, and at-speed flash IP



# Why is JTAG Useful for Debugging?



- "Bare-metal" debugging at the interface between the hardware and the software
- Essential for debug on wedged platforms
- Use same tools as used in silicon validation

### Access Mechanisms (Intel)

XDP (eXtended Debug Port)





DbC/ DCI (Debug Class)



#### CO9 - INTEL SVT DCI DBC2/3 A-TO-A DEBUG CABLE 1.8 METER

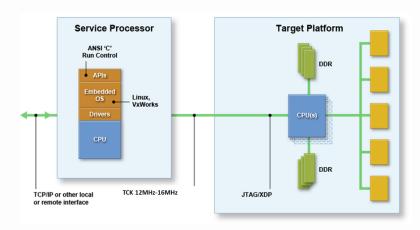
MM#: 955196

Availability: Usually Ships in 24 to 48 Hours

Product Code: ITPDCIAMAM2M

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• BMC

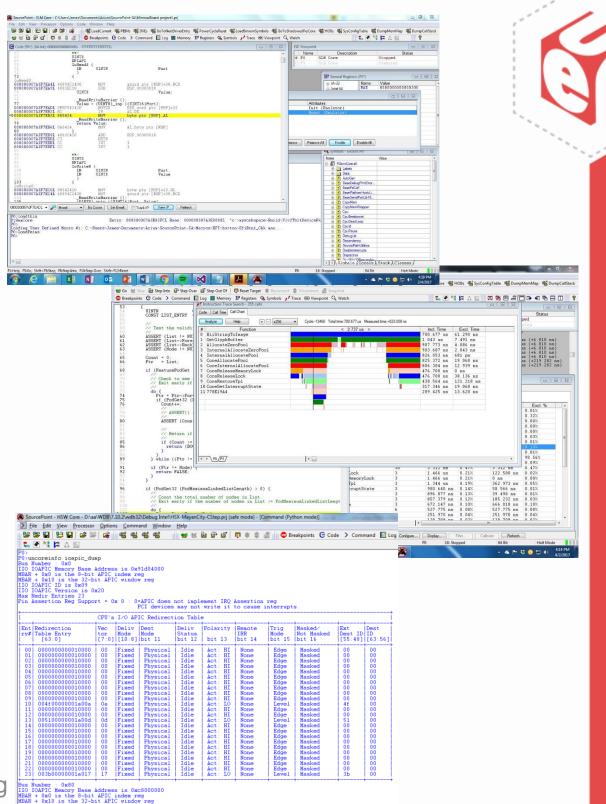


### **Tools of the Trade**

Run-control

Trace

Scripting

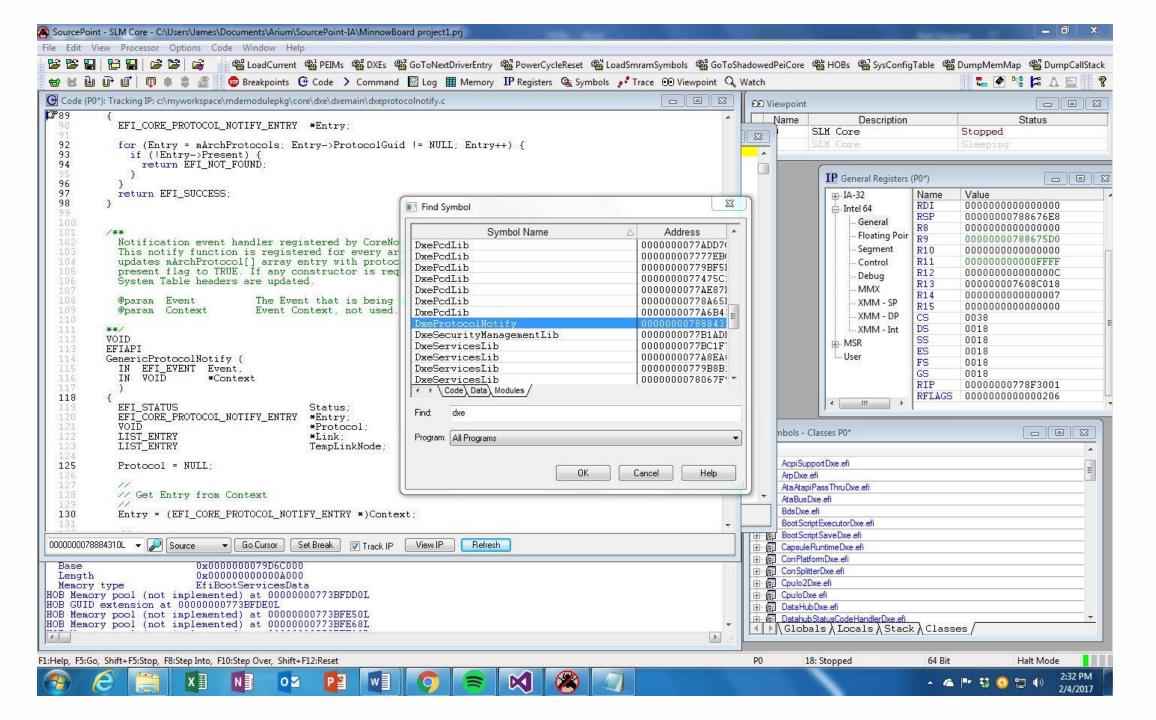




## Examples

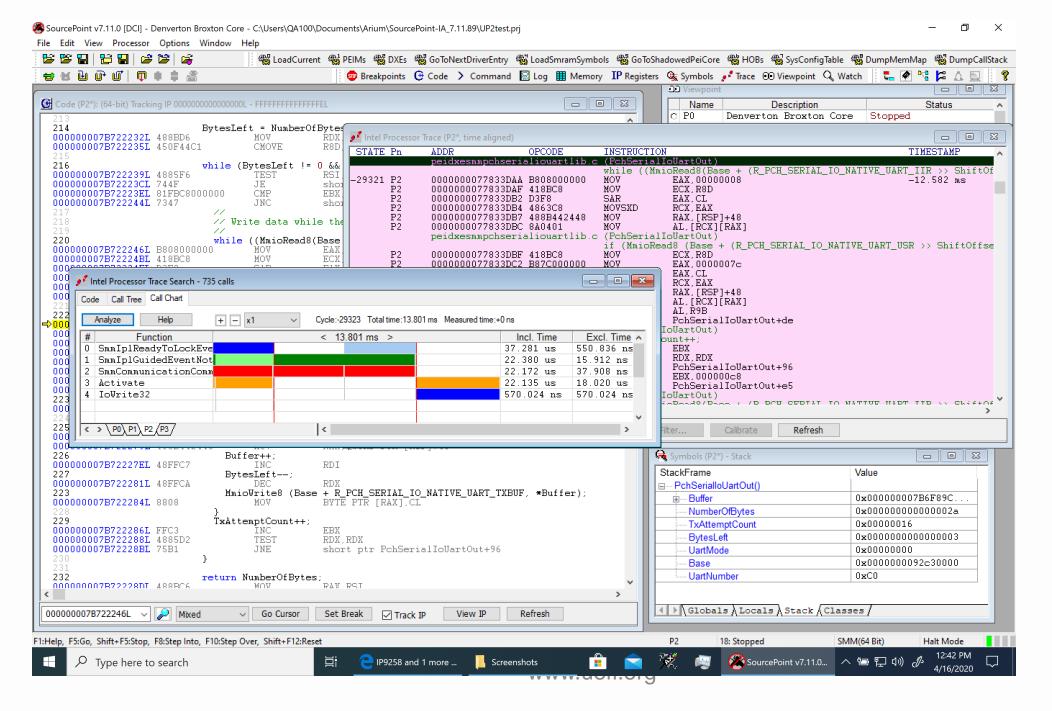
### Basic Run-Control - MinnowBoard



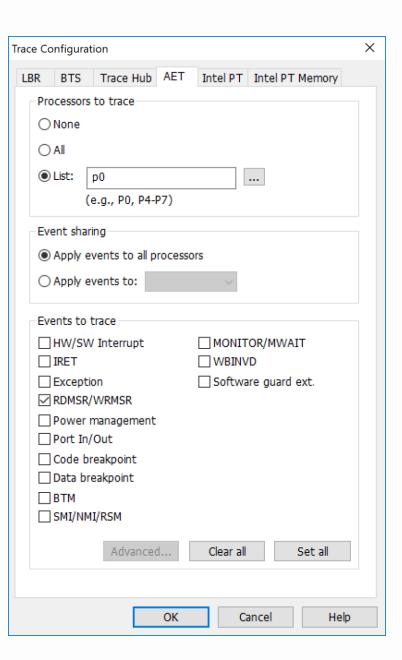


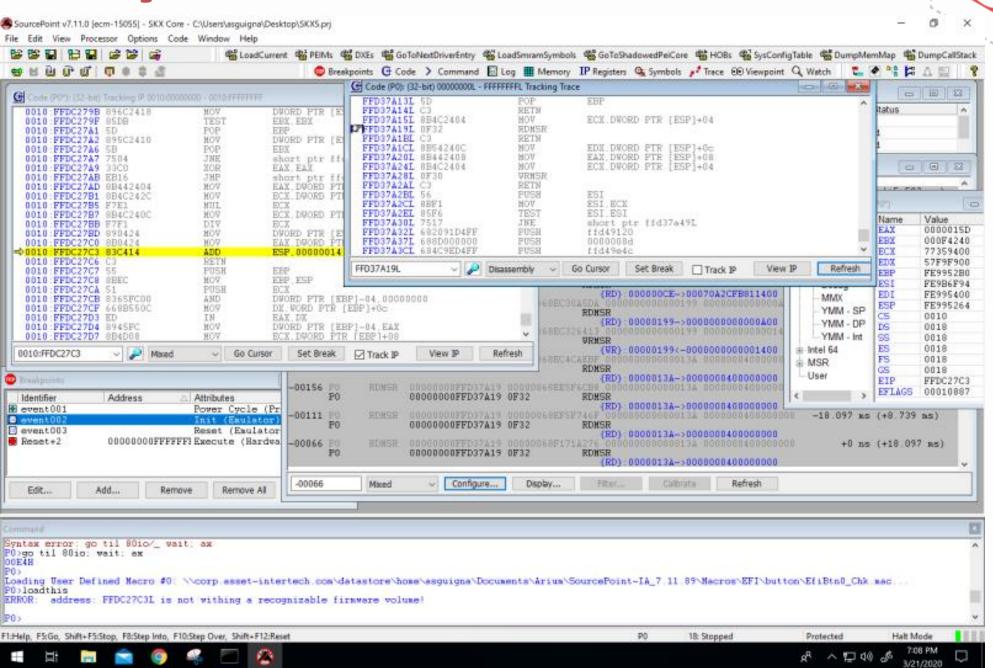
# Intel Processor Trace - Apollo Lake





## Intel AET – Skylake-SP

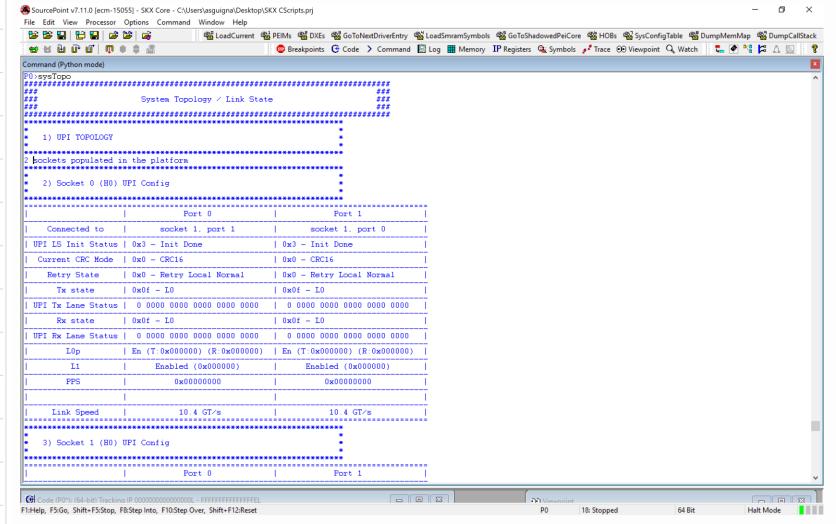




## CScripts - Skylake-SP



bkc	Best Known Configuration checker
coreinfo	Processor Core Information
edk2	UEFI Development Kit 2
ei	Error Injection
error	System Errors
mc	Memory Controller
pch	Platform Control Hub
pci	Peripheral Component Interconnect
pcie	Peripheral Component Interconnect (PCIe) base class
pm	Power Management
ras	Reliability, Availability, Serviceability
skx	Model Specific Registers (MSR)
uncoreinfo	SKX uncore implementation
upi	UPI module implementation



### Call to Action



- Take advantage of open source learning/ development opportunities
  - The MinnowBoard Chronicles
  - Debugging Intel Firmware using DCI & USB3.0
  - -<u>Intel Firmware site</u>



### Questions?

### Thanks for attending the UEFI 2020 Virtual Plugfest

For more information on UEFI Forum and UEFI Specifications, visit <a href="http://www.uefi.org">http://www.uefi.org</a>



